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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/722,218	CHENG ET AL.	
	Examiner	Art Unit	
	Phat X. Cao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The Request for Continued Examination filed on 7/17/08 is acknowledged.

Claim Objections

2. Claim 1 is objected to because of the following informalities: last line, "… at least partially extending above the surface" should be changed to "… at least partially extending above the surface of the substrate". Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. A broad range or limitation together with a narrow range or limitation that falls within the broad range or limitation (in the same claim) (claim 38) is considered indefinite, since the resulting claim does not clearly set forth the metes and bounds of the patent protection desired. See MPEP § 2173.05(c). Note the explanation given by the Board of Patent Appeals and Interferences in *Ex parte Wu*, 10 USPQ2d 2031, 2033 (Bd. Pat. App. & Inter. 1989), as to where broad language is followed by "such as" and then narrow language. The Board stated that this can render a claim indefinite by raising a question or doubt as to whether the feature introduced by such language is (a) merely exemplary of the remainder of the claim, and therefore not required, or (b) a required feature of the claims. Note also, for example, the decisions of *Ex parte Steigewald*, 131 USPQ 74 (Bd. App. 1961); *Ex parte Hall*, 83 USPQ 38 (Bd. App. 1948); and *Ex parte Hasche*, 86 USPQ 481 (Bd. App. 1949). In the present instance, claim 38 recites the broad recitation "first source/drain regions located at least partially within the

substrate … second source/drain regions located at least partially within the substrate", and the claim also recites "one of the first and second source/drain regions is disposed entirely within the substrate, and … one of first and second source/drain regions extends from the surface of the substrate" which is the narrower statement of the range/limitation.

5. Dependent claims 39-43 are also unclear because they depend from unclear independent claim 38.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 5-7, 8-9, 11-12, 15, and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murthy et al (US 2005/0079660) in view of Bohr et al (US 2004/0262683).

Regarding claims 1, 11, and 44, Murthy (Fig. 7) discloses the forming of a semiconductor device comprising: an isolation region 26 located in a bulk silicon substrate 22 (par. [0026]); an NMOS device 20N located partially over a surface of the substrate; and a PMOS device 20P isolated from the NMOS device 20N by the isolation region 26 and located partially over the surface; wherein a first one of the NMOS and PMOS devices 20N/20P includes first source/drain regions 46N/P recessed within the

surface (see Fig. 3 and par. [0030]); and wherein a second one of the NMOS and PMOS devices 20N/20P includes second source/drain regions 46N/P at least partially extending above the surface.

Murthy does not disclose that the first source/drain regions 46N/P of the first one of the NMOS and PMOS devices 20N/20P are disposed entirely below the surface of the substrate.

However, Bohr (Fig. 6) teaches the forming of a semiconductor device, comprising: an isolation region 110 located in a substrate; an NMOS device 603 including first source/drain regions 203 disposed entirely below the surface of the substrate; and a PMOS device 604 isolated from the NMOS device 603 by the isolation region 110, the PMOS device 604 includes second source/drain regions 470/480 at least partially extending above the surface of the substrate. Furthermore, Applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the device would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966). See also MPEP 2144.04(IV).

Therefore, in view of teaching of Bohr, it would have been obvious to modify the device of Murthy by having the first source/drain regions 46N of the NMOS device 20N disposed either above or entirely below the surface of the substrate because changing the dimensions of the first source/drain regions 46N of the NMOS is not critical and these changes produce no functional differences.

Regarding claims 5-7, Murthy does not discloses that one set of the first and second source/drain regions 46N/P comprise SiGe or SiC.

However, Bohr (Fig. 6) teaches the forming of a semiconductor device, comprising: an isolation region 110 located in a substrate; an NMOS device 603 located partially over a surface of the substrate; and a PMOS device 604 isolated from the NMOS device 603 by the isolation region 110 and located partially over the surface, wherein a first one of the NMOS and PMOS devices includes first source/drain regions 470/480 recessed within the surface (see recesses 340 and 360 in Fig. 3) and comprising SiGe or SiC (par. [0024]). Accordingly, it would have been obvious to use SiGe or SiC as a material for at least one set of the first and second source/drain regions 46N/P of Murthy because as taught by Bohr, such materials would create a strain in the channel region of the transistor (par. [0024]), and that strained channel region would increase movement of electrons in NMOS device channel and to increase movement of positive charged holes in PMOS device channel (par. [0002]).

Regarding claims 8-9 and 12, Bohr's Fig. 6 further teaches that the substrate is a bulk silicon substrate having a <110> or <100> crystal orientation (par. [0027], last 5 lines), and the first source/drain regions 470/480 comprises strained source/drain

regions at strain 494 (par. [0026]) for increase movement of positive charged holes in PMOS device channel (par. [0002]).

Regarding claim 15, Bohr also teaches an etch stop layer 663/664 (par. [0039], lines 1-6) located over the NMOS and PMOS devices (Fig. 6) for imparting a first stress in the first source/drain regions 470/480 and a second stress in the second source/drain regions 203, wherein the first and second stresses are substantially different in magnitude (par. [0039]).

8. Claims 2-4, 13-14, 16-22, 24-27, 28-33, 35-37 and 45-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murthy et al and Bohr et al as applied to claims (1 and 44) above, and further in view of Dawson et al (US 5,963,803).

Regarding claims 2, 16, and 45, neither Murthy nor Bohr disclose the PMOS gate having a height greater than a height of the NMOS gate.

However, Dawson (Fig. 1H) teaches a CMOS device comprising: a PMOS gate 122 having a height greater than a height of an NMOS gate 126 (column 7, lines 4-6). Accordingly, it would have been obvious to modify the device of Murthy by forming the PMOS gate having a height greater than a height of the NMOS gate because the relatively high gate for the PMOS device would reduce boron penetration into active region, as taught by Dawson (column 4, lines 32-33).

Regarding claims 3-4, 17, 28, and 46, as discussed above, the combination of Murthy and Bohr substantially reads on the invention as claimed. Bohr's (Fig. 6) further teaches that a first contact 523 coupled to the first source/drain region 203 extends below the surface of the substrate (claim 28).

The combination of Murthy and Bohr does not disclose that the spacers formed on opposing sides of the PMOS gate have a width greater than a width of the spacers formed on opposing sides of the NMOS gate.

However, Dawson (Fig. 1H) teaches a CMOS comprising the spacers 146 formed on opposing sides of the PMOS gate 122 and having a width greater than a width of the spacers 144 formed on opposing sides of the NMOS gate 126 (column 7, lines 4-6). Accordingly, it would have been obvious to modify the device of Murthy by forming the spacers formed on opposing sides of the PMOS gate having a width greater than a width of the spacers formed on opposing sides of the NMOS gate because the relative wide spacers for the PMOS device would offset the rapid diffusion of boron in the source/drain regions for the P-channel device during high temperature processing so that the source/drain regions for the NMOS and PMOS devices would have the desired sizes, as taught by Dawson (column 4, lines 32-40).

Regarding claims 13-14, 18-22, 24-26, 29-33, and 35-36, Bohr (fig. 6) further discloses that the substrate is a bulk silicon substrate having a <110> or <100> crystal orientation (par. [0027], last 5 lines), and the first source/drain regions 470/480 comprises strained source/drain regions made of SiGe or SiC (par. [0024]).

Regarding claims 27 and 37, Bohr also discloses an etch stop layer 663/664 (par. [0039], lines 1-6) located over the NMOS and PMOS devices (Fig. 6) for imparting a first stress in the first source/drain regions 470/480 and a second stress in the second source/drain regions 203, wherein the first and second stresses are different in magnitude (par. [0039]).

9. Claims 10, 23 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murthy et al, Bohr et al, and Dawson et al as applied to claims (16, 28) above, and further in view of Biebl et al (US 5,913,115).

Neither Murthy nor Bohr disclose that the substrate is a silicon-on-insulator substrate.

However, Biebl (Fig. 9) teaches the known feature of forming a PMOS 26 and an NMOS 28 on a surface of a bulk silicon substrate or on a surface of a silicon-on-insulator (SOI) substrate 21 (column 4, lines 45-47). Accordingly, it would have been obvious to modify the device of Murthy by forming the PMOS and NMOS transistors on an SOI substrate because such known SOI substrate would reduce the parasitic effects between the transistors and the substrate.

10. Claim 47 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murthy et al (US 2005/0079660) in view of Bohr et al (US 2004/0262683) and Wuu (US 6,194,258).

Murthy (Fig. 7) discloses the forming of a semiconductor device comprising: an isolation region 26 located in a bulk silicon substrate 22 (par. [0026]); an NMOS device 20N located partially over a surface of the substrate; and a PMOS device 20P isolated from the NMOS device 20N by the isolation region 26 and located partially over the surface; wherein a first one of the NMOS and PMOS devices 20N/20P includes first source/drain regions 46N/P recessed within the surface (see Fig. 3 and par. [0030]); and wherein a second one of the NMOS and PMOS devices 20N/20P includes second source/drain regions 46N/P at least partially extending above the surface.

Murthy does not disclose that the first source/drain regions 46N/P of the first one of the NMOS and PMOS devices 20N/20P are disposed entirely below the surface of the substrate.

However, Bohr (Fig. 6) teaches the forming of a semiconductor device, comprising: an isolation region 110 located in a substrate; an NMOS device 603 including first source/drain regions 203 disposed entirely below the surface of the substrate; and a PMOS device 604 isolated from the NMOS device 603 by the isolation region 110, the PMOS device 604 includes second source/drain regions 470/480 at least partially extending above the surface of the substrate. Furthermore, Applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the device would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966). See also MPEP 2144.04(IV).

Therefore, in view of teaching of Bohr, it would have been obvious to modify the device of Murthy by having the first source/drain regions 46N of the NMOS device 20N disposed either above or entirely below the surface of the substrate because changing

the dimensions of the first source/drain regions 46N of the NMOS is not critical and these changes produce no functional differences.

Neither Murthy nor Bohr specifically disclose a plurality of interconnects connecting to CMOS device.

However, Wuu (Fig. 8) teaches the known feature of connecting a plurality of interconnects 16/18 to CMOS device 70/80. Accordingly, it would have been obvious to provide a plurality of interconnects connecting one of the plurality of CMOS devices of Murthy because such interconnects connections are well known in the art for providing the electrical connections to the CMOS devices.

11. Claims 48-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murthy et al, Bohr et al, and Wuu as applied to claim 47 above, and further in view of Dawson et al (US 5,963,803).

Regarding claim 48, Murthy does not disclose the PMOS gate having a height greater than a height of the NMOS gate.

However, Dawson (Fig. 1H) teaches a CMOS device comprising: a PMOS gate 122 having a height greater than a height of an NMOS gate 126 (column 7, lines 4-6). Accordingly, it would have been obvious to modify the device of Murthy by forming the PMOS gate having a height greater than a height of the NMOS gate because the relatively high gate for the PMOS device would reduce boron penetration into active region, as taught by Dawson (column 4, lines 32-33).

Regarding claim 49, Murthy does not disclose that the spacers formed on opposing sides of the PMOS gate have a width greater than a width of the spacers formed on opposing sides of the NMOS gate.

However, Dawson (Fig. 1H) teaches a CMOS comprising the spacers 146 formed on opposing sides of the PMOS gate 122 and having a width greater than a width of the spacers 144 formed on opposing sides of the NMOS gate 126 (column 7, lines 4-6). Accordingly, it would have been obvious to modify the device of Murthy by forming the spacers formed on opposing sides of the PMOS gate having a width greater than a width of the spacers formed on opposing sides of the NMOS gate because the relative wide spacers for the PMOS device would offset the rapid diffusion of boron in the source/drain regions for the P-channel device during high temperature processing so that the source/drain regions for the NMOS and PMOS devices would have the desired sizes, as taught by Dawson (column 4, lines 32-40).

12. Claims 38-39 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeo et al (US 2004/0173815-previously cited) in view of Murthy et al (US 2005/0079660).

Regarding claims 38, Yeo (Fig. 6F) discloses a semiconductor device, comprising: an isolation region (not shown, see par. [0040]) located in a substrate 500; an NMOS device 5 (par. [0040], last 5 lines) located partially over a surface of the substrate 500; and a PMOS device (par. [0040], last 5 lines) located partially over the surface; wherein the NMOS device 5 includes first source/drain regions 505 located at least partially within the substrate 500 and comprising SiC (par. [0044], lines 22-26);

and the PMOS device 5 includes second source/drain regions 505 located at least partially within the substrate 500 and comprising SiGe (par. [0044], lines 19-22), wherein the first source/drain regions 505 of NMOS device are disposed entirely within the substrate, and wherein the second source/drain regions 505 of PMOS device 5 are extend **downward** from the surface of the substrate (see Fig. 6F).

Yeo does not disclose that both NMOS and PMOS devices 5 formed on a same substrate and isolated from each other by the isolation region.

However, Yeo further discloses that "silicon substrate 500 comprises a previously formed plurality of isolation regions (not shown) and previously defined plurality of device regions" (par. [0040]). Accordingly, it would have been obvious to form both NMOS and PMOS devices 5 on the same substrate 500 and to isolate from each other by the isolation region in order to construct a well-known CMOS device structure, as taught by CMOS device shown in Fig. 7 of Murthy.

Regarding claims 39 and 42, Yeo (Fig. 6F) further discloses the first source/drain regions 505 of NMOS are recessed within the surface (also see Fig. 6D and par. [0043]) and the second source/drain regions 505 of PMOS are recessed within the surface and extend downward from the surface, and wherein at least one set of the first and second source/drain regions 505 comprises strained source/drain regions (par. [0040], last 5 lines).

13. Claim 43 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yeo et al and Murthy et al as applied to claim 38 above, and further in view of Bohr et al (US 2004/0262683).

Neither Yeo nor Murthy disclose an etch stop layer as claimed.

However, Bohr (Fig. 6) teaches an etch stop layer 663/664 (par. [0039], lines 1-6) located over the NMOS and PMOS devices for imparting a first stress in the first source/drain regions 470/480 and a second stress in the second source/drain regions 203, wherein the first and second stresses are different in magnitude (par. [0039]). Accordingly, it would have been obvious to form an etch stop layer over the NMOS and PMOS devices of Yeo because such forming of the etch stop layer would impart the stresses in the first and second source/drain regions, as taught by Bohr.

14. Claims 40-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeo et al and Murthy et al as applied to claim 38 above, and further in view of Dawson et al (US 5,963,803).

Regarding claim 40, neither Yeo nor Murthy disclose the PMOS gate 208 having a height greater than a height of an NMOS gate 208.

However, Dawson (Fig. 1H) teaches a CMOS device comprising: a PMOS gate 122 having a height greater than a height of an NMOS gate 126 (column 7, lines 4-6). Accordingly, it would have been obvious to modify the device of Yeo by forming the PMOS gate having a height greater than a height of the NMOS gate because the relatively high gate for the PMOS device would reduce boron penetration into active region, as taught by Dawson (column 4, lines 32-33).

Regarding claim 41, Yeo does not disclose that the spacers formed on opposing sides of the PMOS gate have a width greater than a width of the spacers formed on opposing sides of the NMOS gate.

However, Dawson (Fig. 1H) teaches a CMOS comprising the spacers 146 formed on opposing sides of the PMOS gate 122 and having a width greater than a width of the spacers 144 formed on opposing sides of the NMOS gate 126 (column 7, lines 4-6). Accordingly, it would have been obvious to modify the device of Yeo by forming the spacers formed on opposing sides of the PMOS gate having a width greater than a width of the spacers formed on opposing sides of the NMOS gate because the relative wide spacers for the PMOS device would offset the rapid diffusion of boron in the source/drain regions for the P-channel device during high temperature processing so that the source/drain regions for the NMOS and PMOS would have the desired sizes, as taught by Dawson (column 4, lines 32-40).

15. Claims 1, 5-7, 8-9, 11-12, 15 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bohr et al (US 2004/0262683) in view of Wieczorek et al (US 6,274,894) – newly cited.

Regarding claims 1, 11, and 44, Bohr (Fig. 6) discloses a semiconductor device comprising: an isolation region 110 located in a substrate; an NMOS device 603 located partially over a surface of the substrate; and a PMOS device 604 isolated from the NMOS device 603 by the isolation region 110 and located partially over the surface; wherein the NMOS 603 of the NMOS/PMOS devices includes first source/drain regions 203 formed within and disposed entirely below the surface of the substrate; and wherein

the PMOS 604 of the NMOS/PMOS devices includes second source/drain regions 470/480 at least partially extending above the surface of the substrate.

Bohr does not disclose that the first source/drain regions 203 of the NMOS are recessed.

However, Wieczorek (Fig. 9) teaches a MOS device having source/drain regions 56 are recessed and disposed entirely below the surface of the substrate. Accordingly, it would have been obvious to modify the device of Bohr by having the first source/drain regions 203 of the NMOS device 603 are recessed because such forming of recessed source/drain regions would reduce diffusion of source/drain regions, would allow allow accurate placement of source/drain regions, and would not cause increased resistances in the MOS device, as taught by Wieczorek (column 5, lines 5-10).

Regarding claims 5-7, Bohr (Fig. 6) further discloses at least one set of the first and second source/drain regions comprising SiGe or SiC (par. [0024]).

Regarding claims 8-9 and 12, Bohr's Fig. 6 further discloses that the substrate is a bulk silicon substrate having a <110> or <100> crystal orientation (par. [0027], last 5 lines), and the first source/drain regions 470/480 comprises strained source/drain regions at strain 494 (par. [0026]) for increase movement of positive charged holes in PMOS device channel (par. [0002]).

Regarding claim 15, Bohr also discloses an etch stop layer 663/664 (par. [0039], lines 1-6) located over the NMOS and PMOS devices (Fig. 6) for imparting a first stress in the first source/drain regions 470/480 and a second stress in the second source/drain

regions 203, wherein the first and second stresses are substantially different in magnitude (par. [0039]).

16. Claims 2-4, 13-14, 16-22, 24-27, 28-33, 35-37 and 45-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bohr et al and Wieczorek et al as applied to claims (1 and 44) above, and further in view of Dawson et al (US 5,963,803).

Regarding claims 2, 16, and 45, neither Bohr nor Wieczorek disclose the PMOS gate having a height greater than a height of the NMOS gate.

However, Dawson (Fig. 1H) teaches a CMOS device comprising: a PMOS gate 122 having a height greater than a height of an NMOS gate 126 (column 7, lines 4-6). Accordingly, it would have been obvious to modify the device of Bohr by forming the PMOS gate having a height greater than a height of the NMOS gate because the relatively high gate for the PMOS device would reduce boron penetration into active region, as taught by Dawson (column 4, lines 32-33).

Regarding claims 3-4, 17, 28, and 46, as discussed above, the combination of Bohr and Wieczorek substantially reads on the invention as claimed. Bohr's (Fig. 6) further teaches that a first contact 523 coupled to the first source/drain region 203 extends below the surface of the substrate (claim 28).

The combination of Bohr and Wieczorek does not disclose that the spacers formed on opposing sides of the PMOS gate have a width greater than a width of the spacers formed on opposing sides of the NMOS gate.

However, Dawson (Fig. 1H) teaches a CMOS comprising the spacers 146 formed on opposing sides of the PMOS gate 122 and having a width greater than a

width of the spacers 144 formed on opposing sides of the NMOS gate 126 (column 7, lines 4-6). Accordingly, it would have been obvious to modify the device of Bohr by forming the spacers formed on opposing sides of the PMOS gate having a width greater than a width of the spacers formed on opposing sides of the NMOS gate because the relative wide spacers for the PMOS device would offset the rapid diffusion of boron in the source/drain regions for the P-channel device during high temperature processing so that the source/drain regions for the NMOS and PMOS devices would have the desired sizes, as taught by Dawson (column 4, lines 32-40).

Regarding claims 13-14, 18-22, 24-26, 29-33, and 35-36, Bohr (fig. 6) further discloses that the substrate is a bulk silicon substrate having a <110> or <100> crystal orientation (par. [0027], last 5 lines), and the first source/drain regions 470/480 comprises strained source/drain regions made of SiGe or SiC (par. [0024]).

Regarding claims 27 and 37, Bohr also discloses an etch stop layer 663/664 (par. [0039], lines 1-6) located over the NMOS and PMOS devices (Fig. 6) for imparting a first stress in the first source/drain regions 470/480 and a second stress in the second source/drain regions 203, wherein the first and second stresses are different in magnitude (par. [0039]).

17. Claims 10, 23 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bohr et al, Wieczorek et al, and Dawson et al as applied to claims (16, 28) above, and further in view of Biebl et al (US 5,913,115).

Neither Bohr nor Wieczorek disclose that the substrate is a silicon-on-insulator substrate.

However, Biebl (Fig. 9) teaches the known feature of forming a PMOS 26 and an NMOS 28 on a surface of a bulk silicon substrate or on a surface of a silicon-on-insulator (SOI) substrate 21 (column 4, lines 45-47). Accordingly, it would have been obvious to modify the device of Bohr by forming the PMOS and NMOS transistors on an SOI substrate because such known SOI substrate would reduce the parasitic effects between the transistors and the substrate.

18. Claim 47 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bohr et al (US 2004/0262683) in view of Wieczorek et al and Wuu (US 6,194,258).

As discussed in details above, the combination of Bohr and Wieczorek substantially reads on the invention as claimed, except that it does not specifically disclose a plurality of interconnects connecting to CMOS device.

However, Wuu (Fig. 8) teaches the known feature of connecting a plurality of interconnects 16/18 to CMOS device 70/80. Accordingly, it would have been obvious to provide a plurality of interconnects connecting one of the plurality of CMOS devices of Bohr because such interconnects connections are well known in the art for providing the electrical connections to the CMOS devices.

19. Claims 48-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bohr et al, Wieczorek, and Wuu as applied to claim 47 above, and further in view of Dawson et al (US 5,963,803).

Regarding claim 48, Bohr does not disclose the PMOS gate having a height greater than a height of the NMOS gate.

However, Dawson (Fig. 1H) teaches a CMOS device comprising: a PMOS gate 122 having a height greater than a height of an NMOS gate 126 (column 7, lines 4-6). Accordingly, it would have been obvious to modify the device of Bohr by forming the PMOS gate having a height greater than a height of the NMOS gate because the relatively high gate for the PMOS device would reduce boron penetration into active region, as taught by Dawson (column 4, lines 32-33).

Regarding claim 49, Bohr does not disclose that the spacers formed on opposing sides of the PMOS gate have a width greater than a width of the spacers formed on opposing sides of the NMOS gate.

However, Dawson (Fig. 1H) teaches a CMOS comprising the spacers 146 formed on opposing sides of the PMOS gate 122 and having a width greater than a width of the spacers 144 formed on opposing sides of the NMOS gate 126 (column 7, lines 4-6). Accordingly, it would have been obvious to modify the device of Bohr by forming the spacers formed on opposing sides of the PMOS gate having a width greater than a width of the spacers formed on opposing sides of the NMOS gate because the relative wide spacers for the PMOS device would offset the rapid diffusion of boron in the source/drain regions for the P-channel device during high temperature processing so that the source/drain regions for the NMOS and PMOS devices would have the desired sizes, as taught by Dawson (column 4, lines 32-40).

Response to Arguments

20. Applicant's arguments with respect to amended claims have been considered but are moot in view of the new ground(s) of rejection.

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (571)272-1703. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571)272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/P. X. C./

/Phat X Cao/
Primary Examiner, Art Unit 2814